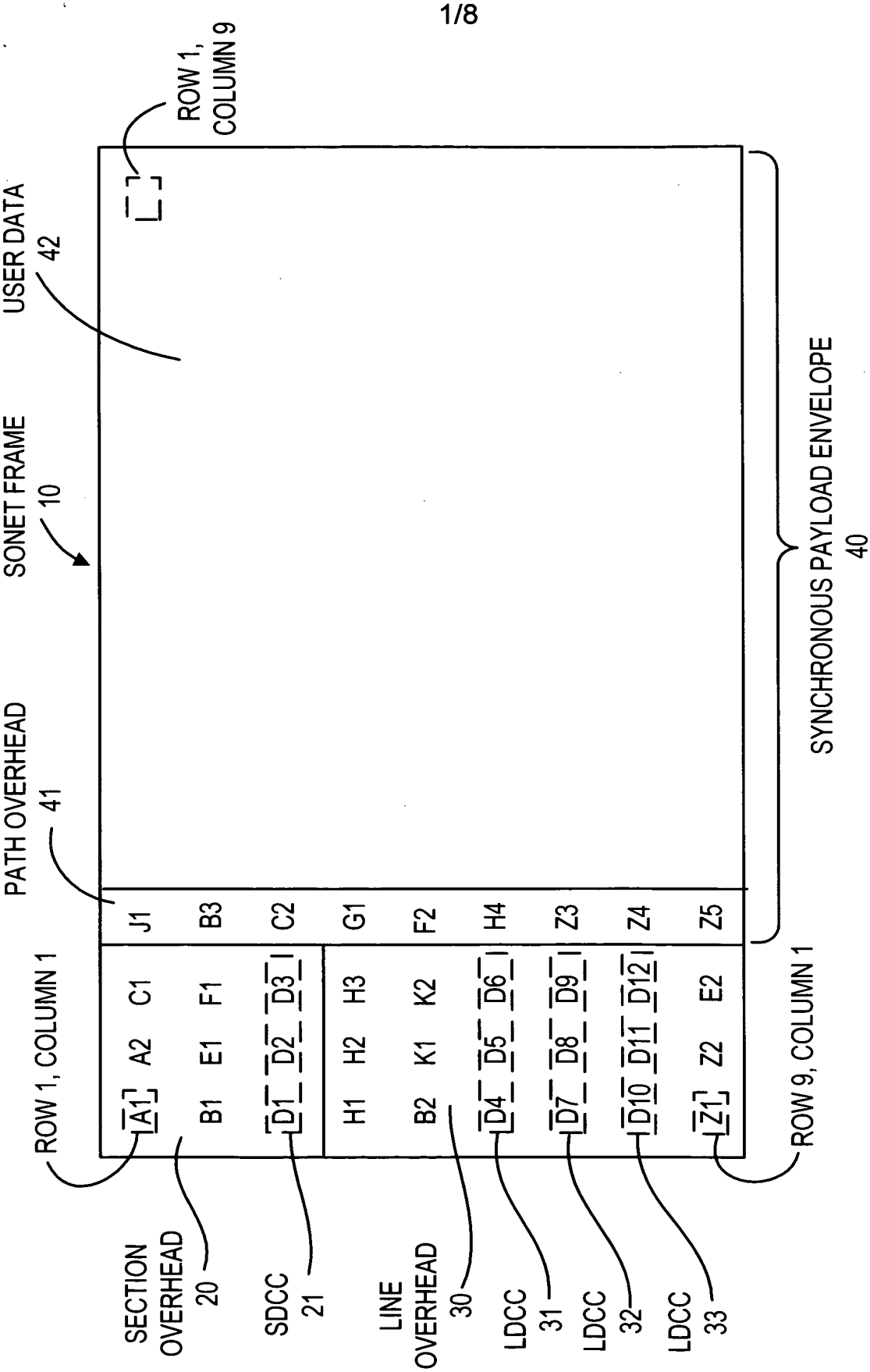
ROW 1, COLUMN 9
USER DATA
42
SONET FRAME
10
PATH OVERHEAD
41
SYNCHRONOUS PAYLOAD ENVELOPE
40
ROW 1, COLUMN 1
ROW 9, COLUMN 1
J1
B3
C2
G1
F2
H4
Z3
Z4
Z5
C1
F1
A2
E1
B1
H3
K2
H2
K1
H1
E2
Z2
A1
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
Z1
SECTION OVERHEAD 20
SDCC 21
LINE OVERHEAD 30
LDCC 31
LDCC 32
LDCC 33

Fig. 1

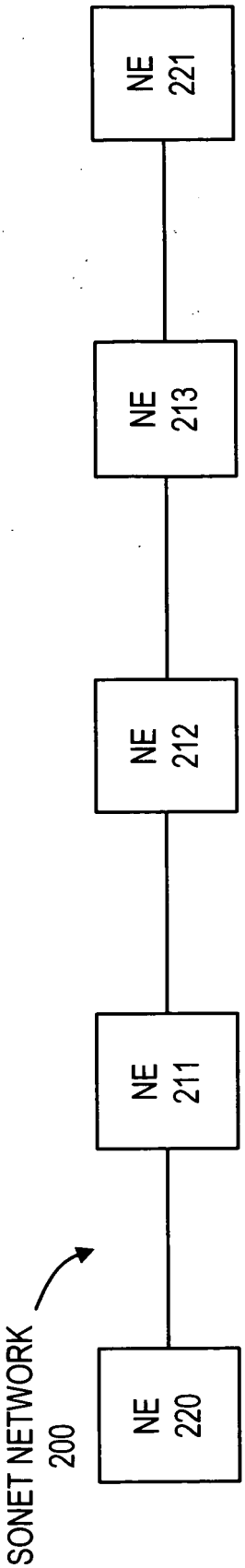
NE 221
NE 213
NE 212
NE 211
NE 220
SONET NETWORK 200

Fig. 2A

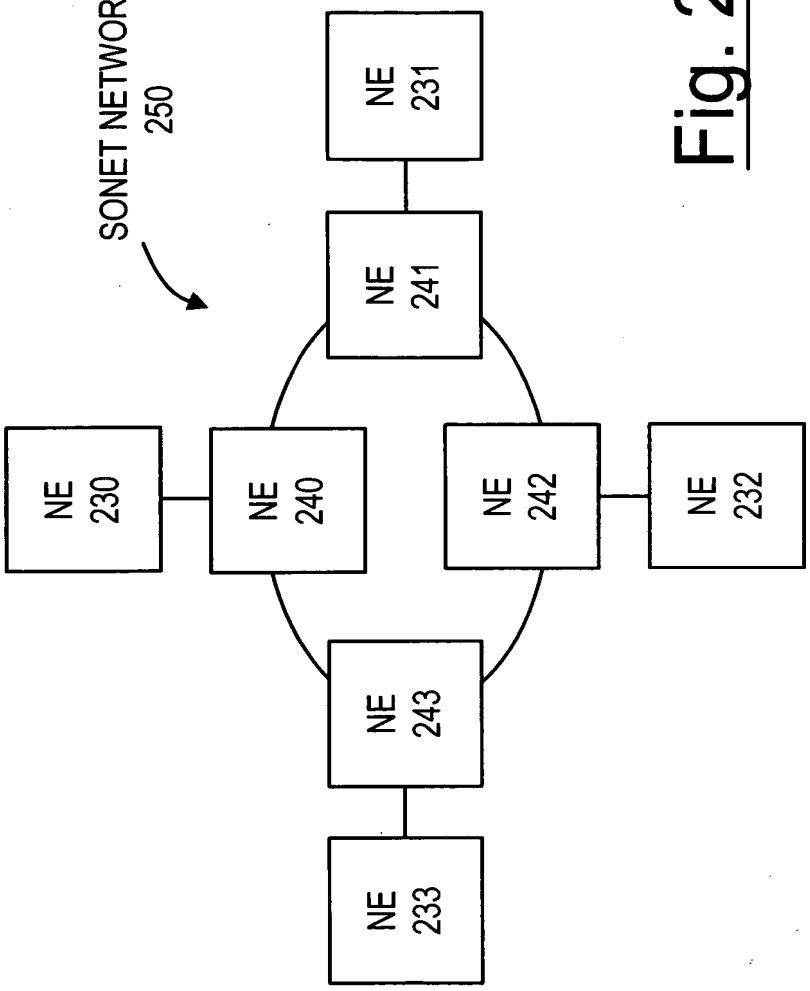
SONET NETWORK 250
NE 231
NE 241
NE 230
NE 240
NE 242
NE 232
NE 243
NE 233

Fig. 2B

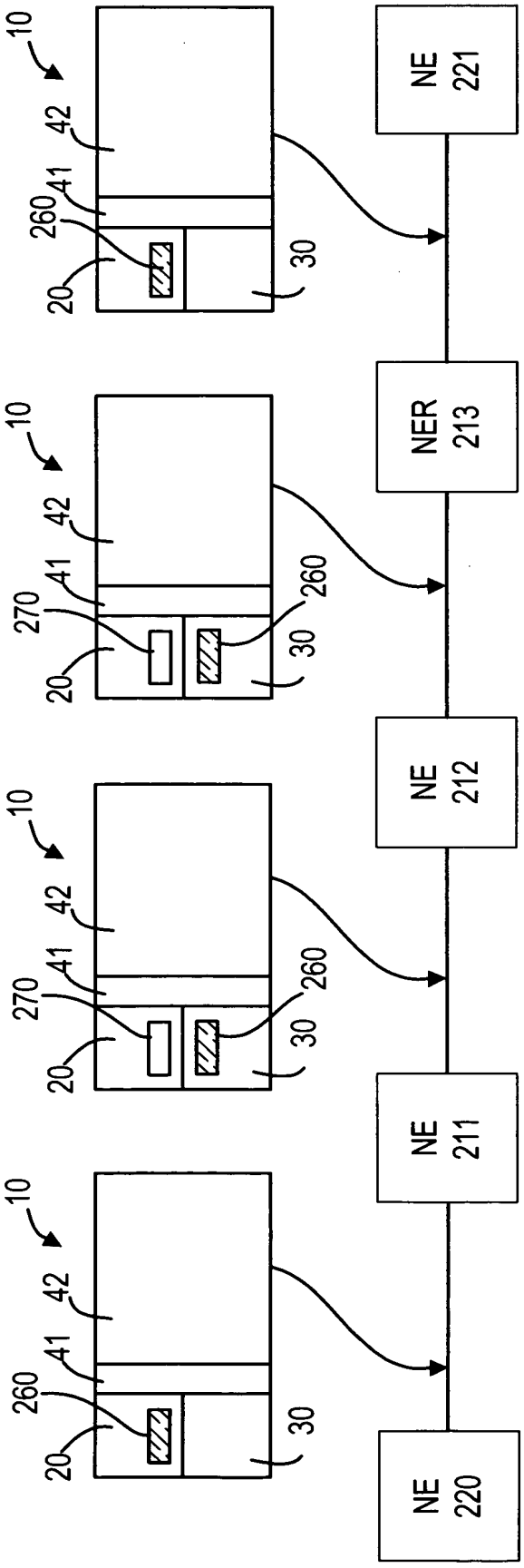
10
42
41
260
20
30
NE 221
NER 213
270
NE 212
NE 211
NE 220
SONET NETWORK 200

Fig. 2C

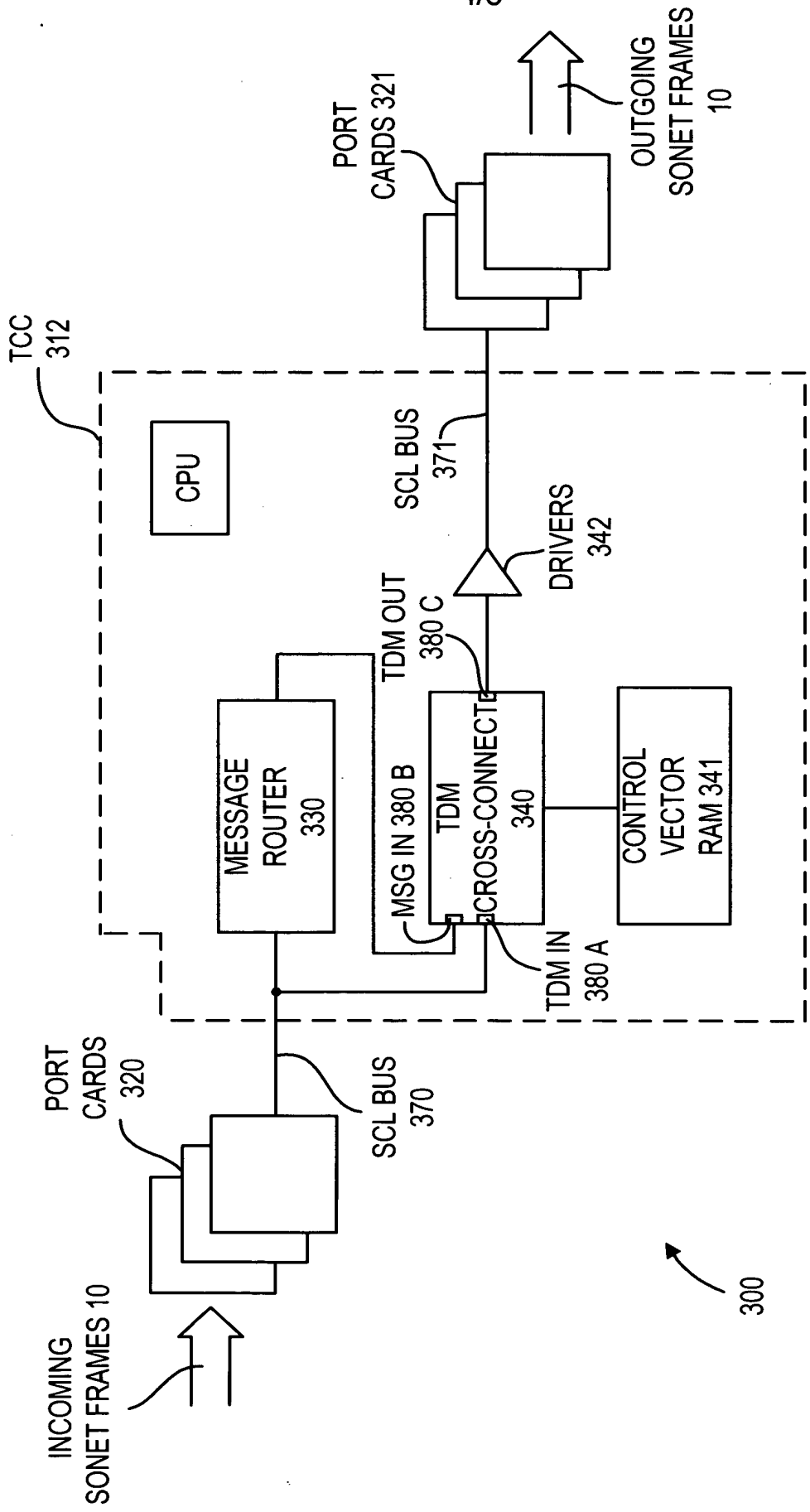
INCOMING SONET FRAMES 10
PORT CARDS 320
SCL BUS 370
TCC 312
CPU
MESSAGE ROUTER 330
MSG IN 380 B
TDM CROSS-CONNECT 340
TDM OUT 380 C
TDM IN 380 A
CONTROL VECTOR RAM 341
DRIVERS 342
SCL BUS 371
PORT CARDS 321
OUTGOING SONET FRAMES 10
300

FIG. 3A

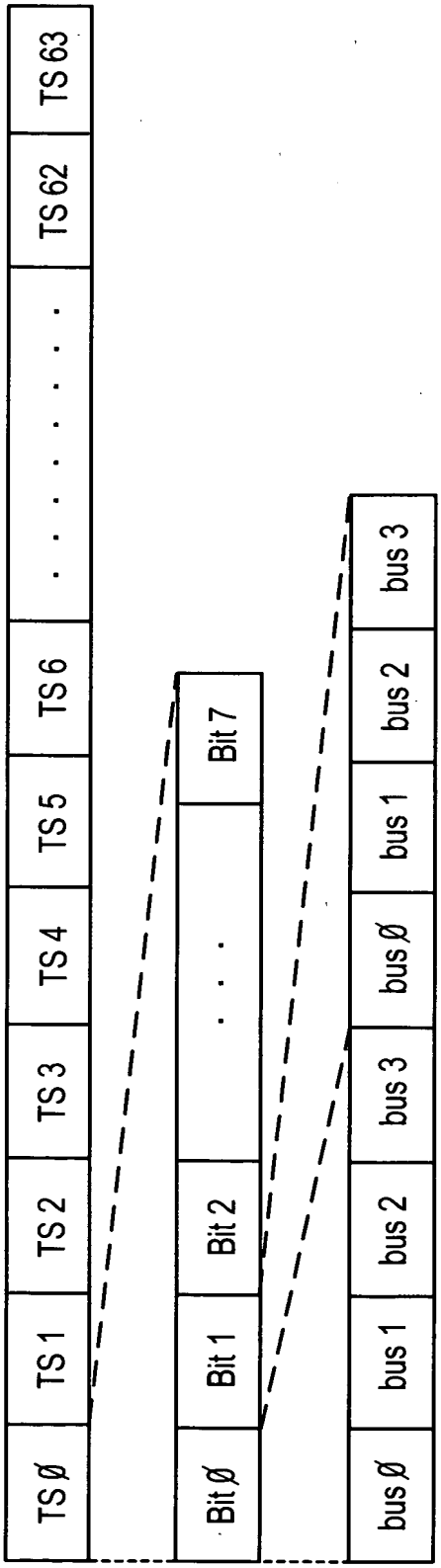
TS Ø
TS 1
TS 2
TS 3
TS 4
TS 5
TS 6
. . . . . .
TS 62
TS 63
Bit Ø
Bit 1
Bit 2
. . .
Bit 7
bus Ø
bus 1
bus 2
bus 3
bus Ø
bus 1
bus 2
bus 3

Fig. 3B

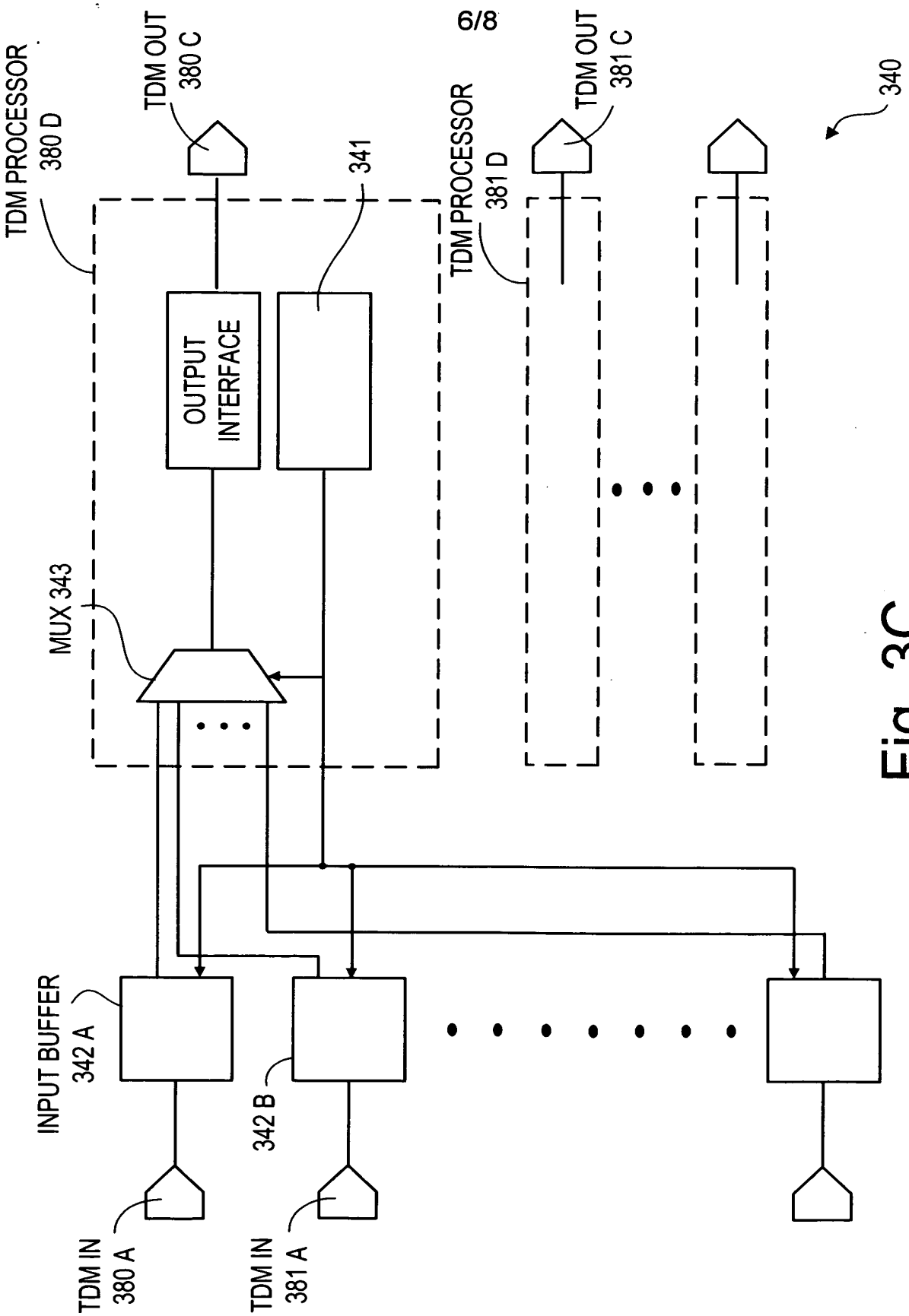
TDM PROCESSOR 380 D
TDM OUT 380 C
341
TDM PROCESSOR 381 D
TDM OUT 381 C
340
OUTPUT INTERFACE
MUX 343
INPUT BUFFER 342 A
342 B
TDM IN 380 A
TDM IN 381 A

Fig. 3C

Patent 6,665,265

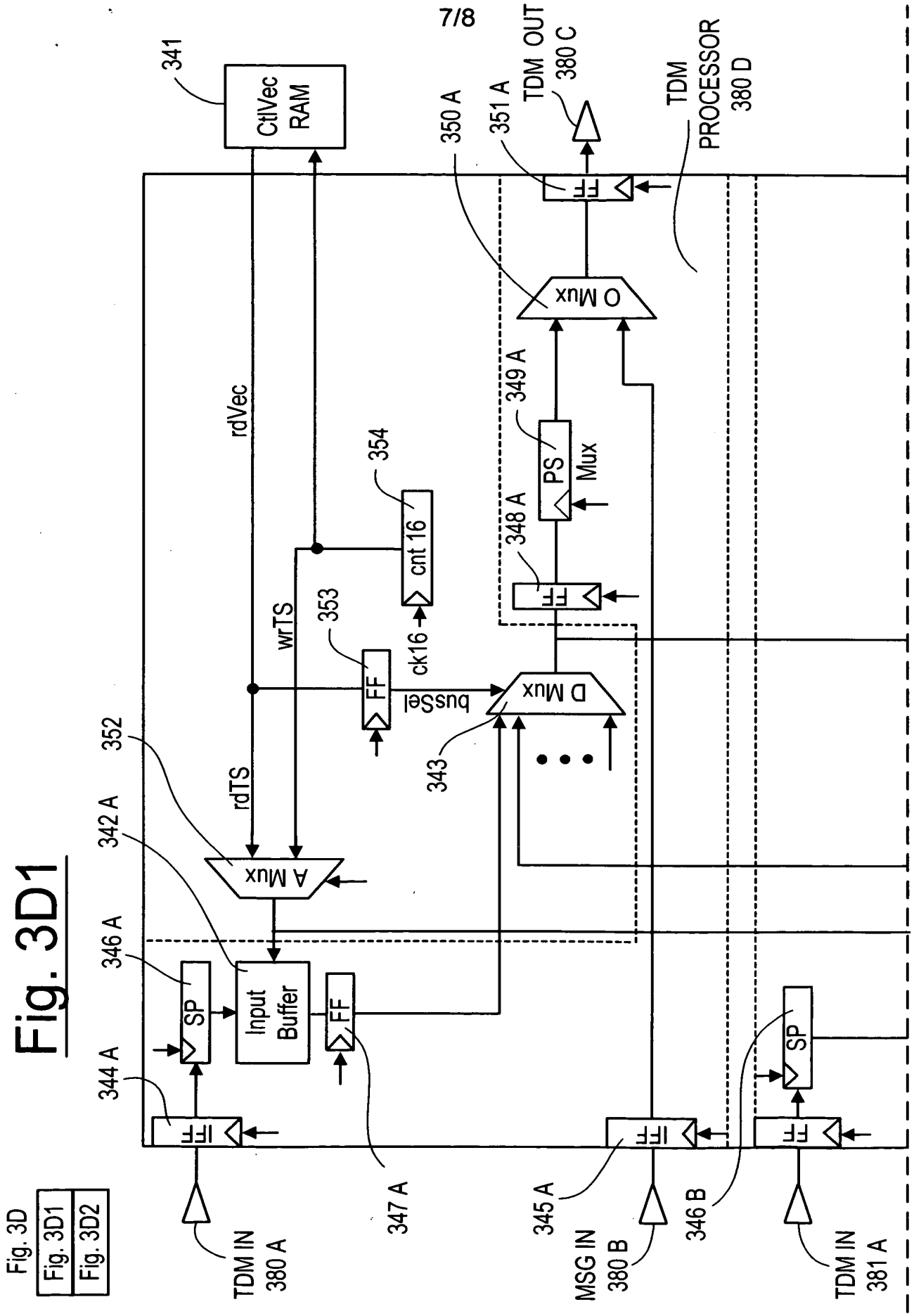

Fig. 3D1

Fig. 3D
Fig. 3D1
Fig. 3D2

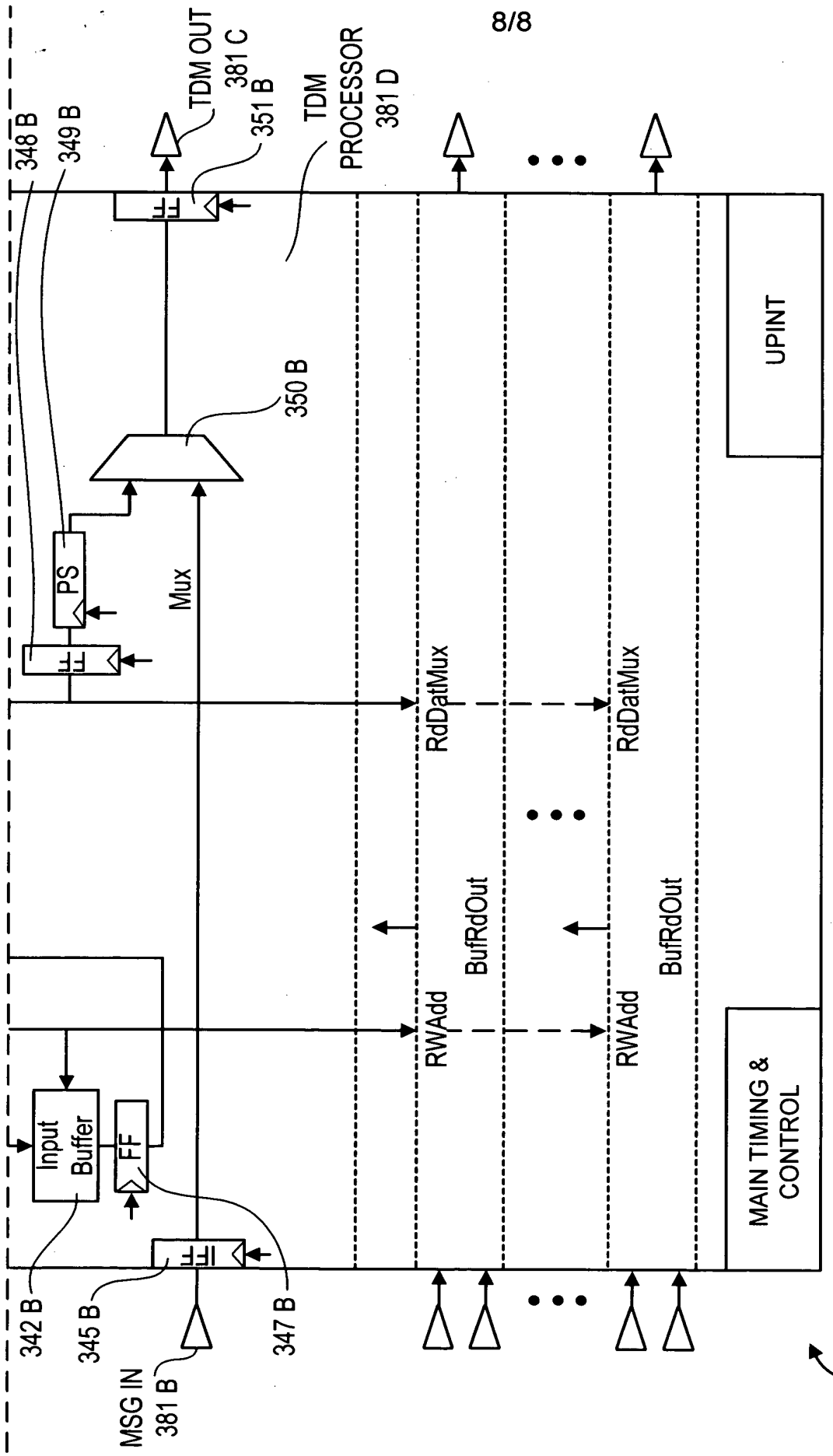
TDM OUT
381 C
351 B
TDM
PROCESSOR
381 D
348 B
349 B
350 B
UPINT
PS
FF
Mux
RdDatMux
RdDatMux
BufRdOut
BufRdOut
RWAdd
RWAdd
Input
Buffer
FF
MAIN TIMING &
CONTROL
342 B
345 B
347 B
MSG IN
381 B
340

Fig. 3D2